

THE ROLE OF CACHE MEMORY IN ENHANCING MICROPROCESSOR PERFORMANCE IN PT. SRIKANDI SINERGI SAKTI

Hendarin¹, Jan Everhard Riwurohi², Setyo Arief Arachman^{3*}
Universitas Budi Luhur, Indonesia
Email: 2411600170@student.budiluhur.ac.id

ABSTRACT

Cache memory in microprocessors has an important role in improving computer system performance by reducing data access time. This research aims to test the hypothesis that increasing the size and level of cache memory can significantly improve microprocessor performance. The research methodology involves a literature study on the concept of cache memory and experimental simulations using computer architecture simulators, such as Gem5, to model scenarios with varying cache sizes and levels. In these simulations, performance parameters such as memory access latency, throughput, and Instructions Per Cycle (IPC) were measured and analyzed. The results show that increasing cache size and level generally contributes towards improving microprocessor performance by reducing data access time. Further statistical analysis supports the hypothesis that there is a positive correlation between cache size and level and system efficiency. These findings provide useful insights in future microprocessor architecture design and memory system optimization.

KEYWORDS Cache Memory, Microprocessor, System Performance, Data Access Time, Computer Architecture Simulation.



This work is licensed under a Creative Commons Attribution-ShareAlike 4.0 International

INTRODUCTION

In the development of computer technology, microprocessors play a very crucial role in determining the overall performance of a computer system (Ma et al., 2015). With the increasing need for increasingly complex computing applications, such as artificial intelligence, graphics processing, and big data processing, the ability of microprocessors to execute instructions quickly and efficiently is becoming increasingly important (Gill et al., 2024). One of the main components that contribute to microprocessor performance is cache memory (Lanka et al., 2024). Cache memory functions as a high-speed storage layer that

How to cite: Hendarin, Jan Everhard Riwurohi, Setyo Arief Arachman. (2024). The Role of Cache Memory in Enhancing Microprocessor Performance in PT. Srikandi Sinergi Sakti. Journal Eduvest. *Vol 4* (12): Page 11824-11829
E-ISSN: 2775-3727
Published by: <https://greenpublisher.id/>

stores data and instructions that are frequently accessed by the processor, thereby reducing access times to slower main memory (RAM) (Hazarika et al., 2020).

Cache memory usually consists of several levels (L1, L2, L3) with different sizes and access speeds. The L1 cache, which is closest to the processor core, has the smallest size but the fastest access, while the L3 cache has a larger size but slower access time. The effectiveness of cache memory in improving microprocessor performance is highly dependent on various factors, including cache size, cache level, and cache management algorithms (cache replacement policies) (Chen et al., 2014). In several previous studies, it has been shown that increasing cache size and optimizing cache architecture can provide significant improvements to processor performance (Mittal & Vetter, 2015). However, the relationship between cache size and level and system performance in various processing scenarios is not fully understood, especially in applications that require intensive memory access (Droliya et al., 2017).

This research focuses on the role of cache memory in improving microprocessor performance by reducing data access time (Adegbija et al., 2017). The main hypothesis proposed is that increasing the size and level of cache memory on a microprocessor will significantly improve system performance. To test this hypothesis, a series of simulation experiments were conducted using computer architecture simulators, such as Gem5, to model various scenarios with varying cache sizes and levels (Brais et al., 2020). Performance parameters such as memory access latency, throughput, and Instructions Per Cycle (IPC) will be measured and analyzed to identify the extent to which increasing cache size and level affects microprocessor performance (Van den Steen et al., 2016).

This research has important contributions in the field of computer architecture, especially in the context of microprocessor design. By understanding the impact of cache size and level on system performance, processor designers can make more informed decisions in determining the optimal cache configuration (Beckmann & Sanchez, 2017). In addition, the results of this research are also expected to provide guidance for software developers in optimizing their applications to utilize cache memory more effectively (Linares-Vasquez et al., 2015).

Furthermore, this research will begin with a literature study to understand the basics of cache memory concepts and its performance. Then, simulation experiments will be conducted to test the proposed hypothesis, followed by statistical analysis to evaluate the performance measurement results. The final results of this research are expected to provide a comprehensive view of the role and optimization of cache memory in improving microprocessor performance.

RESEARCH METHOD

The research methodology includes an in-depth literature study on the concept of cache memory, aiming to understand the role of cache in computer architecture (Zulfa et al., 2020). In addition, experimental simulations are conducted using computer architecture simulators, such as Gem5, to model various scenarios with different cache sizes and levels (Lowe-Power et al., 2020). In the

simulation process, important performance parameters such as memory access latency, throughput, and Instructions Per Cycle (IPC) are measured and analyzed in detail (Hwang et al., 2024). This analysis aims to evaluate how variations in cache size and level affect the overall system efficiency.

RESULT AND DISCUSSION

This research simulates various cache memory sizes and levels to evaluate their impact on microprocessor performance. The computer architecture simulator used is Gem5, with the experimental setup varying the cache size (32KB, 64KB, 128KB, 256KB) and cache level (L1, L2, L3). The measured performance parameters are cache miss rate and Instructions Per Cycle (IPC) as an indicator of microprocessor performance.

1. Results of the Effect of Cache Size on Cache Miss Rate

Table 1 below shows the results of cache miss rate measurements on various cache sizes.

| Ukuran Cache (KB) | L1 Cache Miss Rate (%) | L2 Cache Miss Rate (%) | L3 Cache Miss Rate (%) |
|-------------------|------------------------|------------------------|------------------------|
| 32 | 14.8 | 8.5 | 2.3 |
| 64 | 10.2 | 6.0 | 1.8 |
| 128 | 7.4 | 4.3 | 1.4 |
| 256 | 5.1 | 3.0 | 1.0 |

From Table 1, it can be seen that increasing the cache size significantly reduces the cache miss rate at all cache levels. At 32KB cache size, the cache miss rate is relatively high, especially at L1 (14.8%). However, when the cache size increases to 256KB, the L1 miss rate drops to 5.1%. This shows that increasing the cache size can effectively reduce the miss frequency, thus improving the efficiency of data access.

2. Results of the Effect of Cache Size on IPC (Instructions Per Cycle)

Next, the effect of cache size on IPC was measured to assess the overall performance of the processor. Table 2 displays the results of the IPC measurements at various cache sizes.

Table 2. IPC Based on Cache Size

| Ukuran Cache (KB) | IPC |
|-------------------|-----|
| 32 | 1.8 |
| 64 | 2.4 |
| 128 | 2.9 |
| 256 | 3.2 |

The results in Table 2 show that the increase in cache size is directly proportional to the increase in IPC. As the cache size increases, the processor can

The Role of Cache Memory In Enhancing Microprocessor Performance in PT.
Srikandi Sinergi Sakti

execute more instructions per cycle. At 256KB cache size, the IPC reaches 3.2, which shows an increase in system performance. This is due to the decrease in cache miss rate which allows the processor to access data faster and execute instructions more efficiently.

3. Discussion

The results show that increasing the cache size significantly reduces the cache miss rate and increases the IPC. This is in line with the hypothesis that increasing cache size can improve microprocessor performance. At higher cache levels (L2 and L3), increasing the cache size also has a positive impact with a lower miss rate reduction compared to L1, which has the fastest access time but smaller capacity.

Furthermore, these results confirm the importance of optimal cache design in microprocessor architectures. The right combination of cache size and level is required to achieve a balance between storage capacity and access time. For example, a cache size of 256KB provides the highest IPC in this test, indicating that this size is effective in reducing data access time and increasing system throughput.

However, increasing the cache size has its limits. In this experiment, although increasing the cache size from 128KB to 256KB increases the IPC, larger increments may provide diminishing returns in performance. In addition, larger cache sizes require more power and physical space on the processor, so microprocessor designers should consider these factors when determining the optimal cache configuration (Mittal, 2014).

4. Implications and Suggestions

The findings show that to improve microprocessor performance, there needs to be a balance between cache size and access time. Increasing the cache size up to a certain limit provides advantages in decreased cache miss rate and improved IPC. However, considerations such as power consumption and physical space requirements must be taken into account in the design of the processor architecture. Therefore, further studies can focus on optimizing the cache replacement algorithm and studying its effect on performance in real applications.

CONCLUSION

This research has examined the role of cache memory in improving microprocessor performance by analyzing the effect of cache size and level on cache miss rate and Instructions Per Cycle (IPC). Based on simulation results, it was found that increasing the cache size can significantly reduce the cache miss rate and improve microprocessor performance. Increasing the cache size from 32KB to 256KB shows a decrease in cache miss rate and an increase in IPC, which indicates an increase in the efficiency of data access and instruction execution by the processor.

In addition, the cache level also has an effect on system performance. The L1 cache which has the fastest access time provides greater performance

improvement at the optimal size, while L2 and L3 serve as larger storage with slightly slower access times. These results support the hypothesis that an optimal combination of cache size and level can significantly improve microprocessor system performance.

However, this study also shows that increasing cache size has limitations, such as higher power consumption and physical space requirements on the processor. Therefore, efficient cache design requires a balance between cache size, rate, and access time. The implications of this research emphasize the importance of proper cache management strategies in microprocessor architecture design to achieve optimal performance.

As a suggestion for future research, further exploration of the influence of cache replacement algorithms and their impact on performance in various real applications can be the next step to understand cache optimization in various usage scenarios.

REFERENCES

- Adegbija, T., Rogacs, A., Patel, C., & Gordon-Ross, A. (2017). Microprocessor optimizations for the internet of things: A survey. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 37(1), 7–20.
- Beckmann, N., & Sanchez, D. (2017). Maximizing cache performance under uncertainty. *2017 IEEE International Symposium on High Performance Computer Architecture (HPCA)*, 109–120.
- Brais, H., Kalayappan, R., & Panda, P. R. (2020). A survey of cache simulators. *ACM Computing Surveys (CSUR)*, 53(1), 1–32.
- Chen, X., Chang, L.-W., Rodrigues, C. I., Lv, J., Wang, Z., & Hwu, W.-M. (2014). Adaptive cache management for energy-efficient GPU computing. *2014 47th Annual IEEE/ACM International Symposium on Microarchitecture*, 343–355.
- Droliia, U., Guo, K., Tan, J., Gandhi, R., & Narasimhan, P. (2017). Cachier: Edge-caching for recognition applications. *2017 IEEE 37th International Conference on Distributed Computing Systems (ICDCS)*, 276–286.
- Gill, S. S., Wu, H., Patros, P., Ottaviani, C., Arora, P., Pujol, V. C., Haunschild, D., Parlikad, A. K., Cetinkaya, O., & Lutfiyya, H. (2024). Modern computing: Vision and challenges. *Telematics and Informatics Reports*, 100116.
- Hazarika, A., Poddar, S., & Rahaman, H. (2020). Survey on memory management techniques in heterogeneous computing systems. *IET Computers & Digital Techniques*, 14(2), 47–60.
- Hwang, I., Lee, J., Kang, H., Lee, G., & Kim, H. (2024). Survey of CPU and memory simulators in computer architecture: A comprehensive analysis including compiler integration and emerging technology applications. *Simulation Modelling Practice and Theory*, 103032.
- Lanka, S., Konjeti, P. C., & Pinto, C. A. (2024). A Review: Complete Analysis of the Cache Architecture for Better Performance. *2024 Second International Conference on Inventive Computing and Informatics (ICICI)*, 768–771.
- Linares-Vasquez, M., Vendome, C., Luo, Q., & Poshyvanyk, D. (2015). How

- developers detect and fix performance bottlenecks in android apps. *2015 IEEE International Conference on Software Maintenance and Evolution (ICSME)*, 352–361.
- Lowe-Power, J., Ahmad, A. M., Akram, A., Alian, M., Amslinger, R., Andreozzi, M., Armejach, A., Asmussen, N., Beckmann, B., & Bharadwaj, S. (2020). The gem5 simulator: Version 20.0+. *ArXiv Preprint ArXiv:2007.03152*.
- Ma, K., Zheng, Y., Li, S., Swaminathan, K., Li, X., Liu, Y., Sampson, J., Xie, Y., & Narayanan, V. (2015). Architecture exploration for ambient energy harvesting nonvolatile processors. *2015 IEEE 21st International Symposium on High Performance Computer Architecture (HPCA)*, 526–537.
- Mittal, S. (2014). A survey of architectural techniques for improving cache power efficiency. *Sustainable Computing: Informatics and Systems*, 4(1), 33–43.
- Mittal, S., & Vetter, J. S. (2015). A survey of architectural approaches for data compression in cache and main memory systems. *IEEE Transactions on Parallel and Distributed Systems*, 27(5), 1524–1536.
- Van den Steen, S., Eyerman, S., De Pestel, S., Mechri, M., Carlson, T. E., Black-Schaffer, D., Hagersten, E., & Eeckhout, L. (2016). Analytical processor performance and power modeling using micro-architecture independent characteristics. *IEEE Transactions on Computers*, 65(12), 3537–3551.
- Zulfa, M. I., Hartanto, R., & Permanasari, A. E. (2020). Caching strategy for Web application—a systematic literature review. *International Journal of Web Information Systems*, 16(5), 545–569.